REMARKS/ARGUMENTS

Amendments were made to the specification to correct errors and to clarify the specification. No new matter has been added by any of the amendments to the specification.

Claims 1-27 are pending in the present application. Claims 2-8, 12-13, 15-20, 23-24, and 26-27 were canceled; claims 1, 9, 14, 21, and 25 were amended. Reconsideration of the claims is respectfully requested.

I. Objection to the Specification

The Examiner objected to the specification because of an informality on page 2, line 8. Applicants have amended the specification to correct this informality. Therefore, this objection has been overcome and should be withdrawn.

II. Objection to Claims

The examiner has objected to claims 1, 14, and 25 because of the following informalities:

> In phrase "a memory card, said memory card,", "said memory card," is redundant and should be removed. Appropriate correction is required.

The examiner has objected to claim 13 because of the following informalities:

> Claim 13 is objected to because it appears that this claim should be dependent on claim 2 and not claim 12.

Office Action dated March 30, 2007, page 2.

Applicants have amended claims 1, 14, and 25 to correct the informality, and Applicants have canceled claim 13. Therefore, these objections have been overcome and should be withdrawn.

III. 35 U.S.C. § 101

The Examiner has rejected claims 25-27 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter.

The Examiner states:

> **Claims 25-27** are rejected under 35 U.S.C. 1 01 because the claimed invention is directed to non-statutory subject matter. These claims recite a computer program product in a data processing system, but are not stored on a tangible computer readable medium.

Office Action dated March 30, 2007, pages 2-3.

Applicants have amended claim 25 to recite: "A computer program product that is stored on a tangible computer readable medium..." In addition, Applicants have amended the specification to cancel the language regarding "transmission-type media".

Thus, the rejection of claims 25-27 under 35 U.S.C. § 101 has been overcome and should be withdrawn.

IV. Claim Amendments

Applicants have amended the independent claims to recite similar features. Claim 1 is representative of these claims.

Claim 1 recites:

said memory system including a memory card, a plurality of physical dual inline memory modules (DIMMs) that are attached to said memory card, and a memory controller for controlling said memory card; (Support can be found in the specification page 7, lines 7-9.)

said memory card coupled to said memory controller using a JTAG bus, said memory card including a plurality of empty slots to which additional physical DIMMs can be attached, and said memory card including a plurality of electrical buffers that are part of said memory card; (Support can be found in Figure 2, # 234, on page 6, lines 29-32; and page 14, lines 15-18.)

testing said plurality of physical DIMMs first using a physical DIMM test; (Support can be found in the specification on page 6, lines 24-26.)

responsive to no error occurring during said physical DIMM test, testing said memory card using a memory card test; (Support can be found in the specification on page 6, lines 24-26; and page 7, lines 7-10.)

responsive to no error occurring during said memory card test, testing said memory controller next using a memory controller test; (Support can be found in the specification on page 6, lines 24-26.)

responsive to said memory controller passing said memory controller test, determining that said memory system is good; (Support can be found in the specification on page 9, lines 4-6.)

utilizing said plurality of electrical buffers as a virtual memory controller when testing said plurality of physical DIMMs, and utilizing said plurality of electrical buffers as virtual physical DIMMs when testing said memory card; (Support can be found in the specification on page 6, line 31, through page 7, line15.)

coupling said plurality of electrical buffers to a service processor using a JTAG bus, said service processor controlling said plurality of electrical buffers using said JTAG bus; (Support can be found in the specification on page 7, lines 2-4; and page 11, lines 11-15.)

said physical DIMM test including:

scanning DIMM test data and address information to said plurality of electrical buffers, which then scan said DIMM test data to all addresses in each one of said plurality of physical DIMMs; (Support can be found in the specification on page 6, lines 27-29; and page 17, lines 17-19.)

reading data from said plurality of physical DIMMs; (Support can be found in the specification on page 17, line 32, through page 18, line 2.)

scanning, from said plurality of electrical buffers, said data that was read from said plurality of physical DIMMs; (Support can be found in the specification on page 18, lines 2-4.)

determining that said plurality of physical DIMMs passed said physical DIMM test if said data that was read from said plurality of physical DIMMs matches said DIMM test data; (Support can be found in the specification on page 18, lines 8-10.)

said memory card test including:

assigning a unique identifier to each one of said plurality of electrical buffers, each one of said plurality of electrical buffers addressable by the service processor using said unique identifier; (Support can be found in the specification on page 7, lines 17-19.)

treating each one of said plurality of electrical buffers as a virtual physical DIMM; (Support can be found in the specification on page 7, lines 19-24.)

testing, by the service processor, data bits by writing card test data to each memory location in said virtual physical DIMM, and then reading data from each memory location in said virtual physical DIMM; (Support can be found in the specification on page 7, lines 23-31.)

if said data that was read from said virtual physical DIMM matches said card test data, performing address bit verification on said memory card; (Support can be found in the specification on page 7, lines 28-31.)

said address bit verification to test address bits including:

writing a known test pattern to a first memory location that falls within a range of said virtual physical DIMM, and then reading a set of addresses that fall within said range of said virtual physical DIMM; (Support can be found in the specification on page 8, lines 5-12.)

determining whether said known test pattern was read from only said first memory location; (Support can be found in the specification on page 8, lines 7-12.)

if said known test pattern was read from only said first memory location: said service processor determining that said memory card passed said address bit verification for said first memory location, removing said known test pattern from said first memory location, and performing said address bit verification on a next memory location; and(Support can be found in the specification on page 8, lines 12-19.)

if all memory locations that fall within said range pass said address bit verification, determining that said memory card passed said memory card test. (Support can be found in the specification on page 8, lines 12-19.)

V. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1, 14 and 25 under 35 U.S.C. § 102(e) as being anticipated by *Cox*, Serial Architecture for Memory Module Control, U.S. Patent No. 5,357,621, dated October 18, 1994 (hereinafter referred to as "*Cox*"). This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Applicants have incorporated the features of claims 2, 15, and 26 into claims 1, 14, and 25, respectively. Because the Examiner found that *Cox* does not teach the features of claims 2, 15, and 26, Applicants' claims 1, 14, and 25 are not anticipated by *Cox*. Therefore, this rejection has been overcome and should be withdrawn.

VI. 35 U.S.C. § 103, Obviousness

The Examiner has rejected claims 2-13, 15-24 and 26-27 under 35 U.S.C. § 103(a) as being unpatentable over *Cox* in view of *James* et al., Computer System Configuration Via Test Bus, U.S. Patent No. 5,343,478, dated August 30, 1994 (hereinafter referred to as "*James*"). This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Cox teaches plug-in memory modules 20 that are coupled to a memory system controller. Memory modules 20 are plug-in modules. *Cox* provides an expandable memory system where the total capacity of the system can be increased or changed by plugging in or removing memory modules. Each memory module includes memory blocks 1 and 2. Each memory block comprises a 256 Kbyte DRAM memory array.

Regarding claims 1, 14, and 25, the Examiner stated:

> Cox teaches a memory system (MCL system, **Fig.** 1) includes a plurality of components, said plurality of components including a physical memory module (memory block 1, **Fig.** 1) coupled to a memory card (memory module **20, Fig. 1),** said memory card, and a memory controller (MCL Controller 13, **Fig.** 1) for controlling said memory card, and logic (MCL System Controller 11, **Fig.** 1) that tests each one of said plurality of components separately to identify a defective one of said plurality of components. (Col. 3, 11. 23-27, col. **4,** 11. 58-62, col. 10, 1. 60 to col. 11, **1.** 7).

Office Action dated March 30, 2007, page 3.

Applicants have amended the claims to describe a plurality of physical dual inline memory modules (DIMMs). A "DIMM" is defined by Microsoft Computer Dictionary, Fifth Edition, published

2002, as "Acronym for dual inline memory module. A type of memory board comprised of RAM chips mounted on a circuit board, similar to the more commonly used SIMM (Single Inline Memory Module)..." Thus, a DIMM is a memory board.

The Examiner asserts that the memory blocks of *Cox* are analogous to the memory modules originally recited in Applicants' claims. Applicants have amended the claims to recite physical DIMMs. The memory blocks of *Cox* are not physical DIMMs because the memory blocks are not a type of memory board comprised of RAM chips mounted on a circuit board.

Applicants have also amended the claims to describe the physical DIMMs being attached to the memory card. The memory card includes a plurality of empty slots to which additional physical DIMMs can be attached. Applicants claim a memory controller for controlling the memory card. The memory card is coupled to the memory controller using a JTAG bus.

The Examiner asserts that the memory module 20 of *Cox* is analogous to the memory card claimed by Applicants. The Examiner also asserts that MCL Controller 13 is analogous to the memory controller claimed by Applicants. Applicants disagree.

The memory card claimed by Applicants includes empty slots to which additional DIMMs can be attached. The memory module 20 of *Cox* does not include empty slots to which a DIMM can be attached. The memory card claimed by Applicants is coupled to the memory controller using a JTAG bus. The memory module 20 of *Cox* includes the MCL Controller 13.

Cox does not teach the memory modules 20 being attached to a memory card that is coupled to the central memory controller 11, where the memory card itself and central memory controller 11 are tested. *Cox* does not teach such a memory card that includes electrical buffers that are part of the memory card.

The Examiner admits that *Cox* provides no teaching regarding the order of testing. The Examiner relies on *James* to cure the deficiencies of *Cox*. Primarily, the Examiner relies on Figure 13, and columns 12-13, of *James*. Figure 13 depicts instruction error detection for a configuration and test bus.

James does not teach memory modules that are attached to a memory card that is coupled to a memory controller, where the memory card includes electrical buffers as part of the card. *James* also does not teach testing physical DIMMs first using a physical DIMM test; responsive to no error occurring during said physical DIMM test, testing said memory card using a memory card test; responsive to no error occurring during said memory card test, testing said memory controller next using a memory controller test; and responsive to said memory controller passing said memory controller test, determining that said memory system is good.

Neither *Cox* nor *James* teaches utilizing electrical buffers that are part of the memory card as a virtual memory controller when testing said plurality of physical DIMMs, and utilizing the electrical

buffers as virtual physical DIMMs when testing said memory card, wherein said plurality of physical DIMMs are not tested when testing said memory card.

For the reasons given above, Applicants believe the claims are not rendered obvious by the combination of *Cox* and *James*.

VII. Conclusion

It is respectfully urged that the subject application is patentable over *Cox* and *James* and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: June 29, 2007

Respectfully submitted,

/Lisa L.B. Yociss/

Lisa L.B. Yociss
Reg. No. 36,975
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Attorney for Applicants